The output of the summer must contain a clipping circuit to cause the output data to saturate rather than wrap around in the event that the summation causes the value to exceed the number of bits available in the output path.

The synthetic aperture circuit is also required to be able to subtract the incoming data from a PRI which was acquired previously or to subtract the previous data from the incoming PRI. The addition/subtraction selection will be done on a PRI to PRI basis.

The synthetic aperture circuit must be capable of passing data through unaltered.

2.3.5 Quadrature Bandpass (QBP) Filter

The QBP filter requires two separate filters that operate independently on the single incoming data stream for each of the IFOM's data paths. One of the filters produces the Inphase signal and the other produces the Quadrature signal. By using otherwise identical coefficients that are 90 degrees out of phase, these two filters produce data streams that are 90 degrees out of phase.

2.3.5.1 Decimation Range

The filter must also be a decimating filter. The required decimation range is from one to a maximum of [redacted] The QBP filter will be capable of a decimation rate of one, where the output rate is the same as the input rate. This is desirable for echo modes and possibly color Doppler as well. The maximum decimation rate of [redacted] is used realistically for CW Doppler only. For all other modes, the maximum required decimation rate will be less than or equal to [redacted]

2.3.5.2 Filter Length

Each section of the QBP filter must contain at least 12 multiplier accumulators (MACs). The maximum possible length of the filter which can be implemented will then be equal to [redacted] times the decimation rate. This relationship will be valid up to the decimation rate of [redacted] where the maximum length of [redacted] taps will be achieved. At that point, the filter length can remain constant as the decimation rate increases.

The data path through the QBP filter will be 16 bits wide. The coefficients must be at least 12 bits wide.

2.3.5.3 Shifter

In order to make the most use of the full 12 bits, the QBP filter must allow for gain to be applied to the coefficients so that they have 12 bits of precision. To do this, the accumulators in the MACs must include at least [redacted] additional bits beyond the [redacted] required by the [redacted] x [redacted] multipliers. Then, the accumulators must be followed by a shifter to effectively divide the result in order to compensate for the gain applied to the coefficients.

The coefficient gain, and hence the amount of shift necessary to compensate, will be constant for all filters applied to a PRI.

The shifter must also be accompanied by a clipping circuit to prevent the output from wrapping around in the event that the coefficient's gain is too great or if the output shift value is inadequate.

2.3.5.4 Filter Select

The QBP filter must be programmable to be able to execute one of four possible filters on a PRI to PRI basis. The filter must be capable of being programmed to perform any filter within its operating constraints, but only four sets of parameters need to be available at any one time.

Selecting amongst the filters will be done by a field in the process control header that precedes data for each line on the RF bus. The AIFOM is also required to use this same header field to select amongst the sets of coefficients which must be available at any time.

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The data which enters the Norm/Sum ASIC is 18 bits wide. This amount of precision will be maintained through the summation process and in the buffer RAMs. A clipper in the Norm/Sum ASIC will prevent wraparound if the summation process causes the data to grow beyond [redacted] bits. The data width must be reduced to [redacted] bits before being sent to the downstream filters. This will be done simply by truncating the data as it comes out of the Norm/Sum ASIC. Only the [redacted] most significant bits will be connected to the downstream circuits.

Passing of AQ Bus Headers:

The controller for the SA circuit controls the data path through this circuit. It must therefore receive the RF bus qualifiers, or some other indicator, to know when the AQ bus headers are arriving onto the AIFOM. It should then control the data path to pass the headers through without any normalization or summation and indicate to the downstream circuits that valid headers are arriving.

5.3.7 QBP Filter

The Quadrature Bandpass Filter will be designed using one of the new MuRF ASICs for each of the I and Q channels. The MuRF implements [redacted] separate FIR filters with integral delays of coefficients between the filters for programmable decimation. Refer to the MuRF Source Control Document for more information on this chip.

5.3.7.1 QBP Filter Control

The MuRF chip is controlled by loading it with parameters for filter length, decimation rate and output shift value. Additional flexibility is available for shutting off selected MACs to allow for an odd number filter taps or to extend the effective length of the delay FIFOs. The MuRF contains four sets of control registers which allows it to have up to four different sets of filter parameters available at any point in time. Prior to processing each PRI, one of the four sets will be selected by a pair of bits which are the output of a look up table. The pointer into the look up table will be the Filter Select field of the RF bus process control header.

The AIFOM's MOP will be connected to the control port on all of the MuRF chips on the board. Therefore the MOP will be able to write and read the control registers inside the MuRF. The MOP will be responsible for loading the control registers with the appropriate values for implementing the desired filter.

The MuRF chips will also receive two additional signals from controllers located farther upstream in the data path. One signal will be Filter Start/Stop, which can also be thought of as filter reset. This signal will go to the Stop position at the end of processing each PRI. After the header, and therefore the new filter select code, for the next PRI has been received but before data begins to arrive the Filter Start/Stop bit will go to the start position. The MuRF should then be ready to filter the next PRI of data. The MuRF will also be given a Data Valid strobe. This signal will be synchronous with the RF Bus clock and will be active for each clock during which incoming data is valid. The MuRF will throttle itself so that it processes only when the Data Valid strobe is active.

The QBP filter section will contain a separate control circuit for coordinating the operation of the MuRF and the coefficient address generator. This controller will be responsible for delaying the data valid and possibly the data to the MuRF but not to the coefficient address generator. This may be necessary in order to compensate for pipeline delays through the coefficient generation circuit so that associated data and coefficients arrive at the MuRF at the same clock cycle. This circuit will also be responsible for coordinating the delay of filter start and coefficient start when the two AIFOM channels are used to extend the QBP filter length. In this mode it is necessary to delay the start of one channel by one half the decimation rate.

The MuRF will also send out an Output Data Valid strobe when it has a filtered output ready. This strobe will be used by downstream processors to know when to accept data from the